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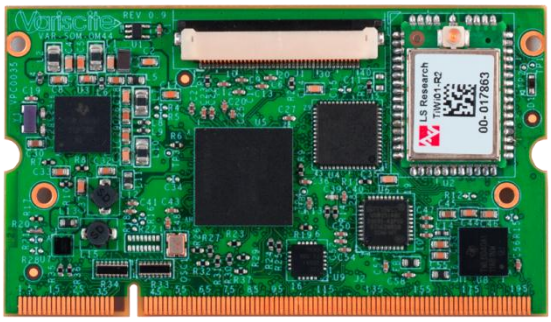
VAR-SOM-OM44 V1.1 Datasheet

Texas Instruments OMAP4™-based System-on-Module

Data Sheet Rev: 1.2



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VAR-SOM-OM44 Datasheet

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Document Revision History

Revision		Date	Notes
PCB	**Data Sheet**		
0.9	**1.0**	22/09/2011	Initial
	1.1	13/11/2011	Adding preliminary power consumption data " Table 3.2, SO-DIMM 200 Pin Mux update Table 4.3.2, CPI signals update Adding reference for GPMC/JTAG connector mating cable.
1.1	**1.2**	1/3/2012	Power consumption update (now Tables 7.3.1 & 7.3.2) Adding Wi-Fi Module description Adding Heat spreader data DSI Support updated MMC Electrical characteristics update

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1 Overview

1.1 General Information

The VAR-SOM-OM44 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, the VAR-SOM-OM44 secures an Intel Atom performance level.

Supporting products:

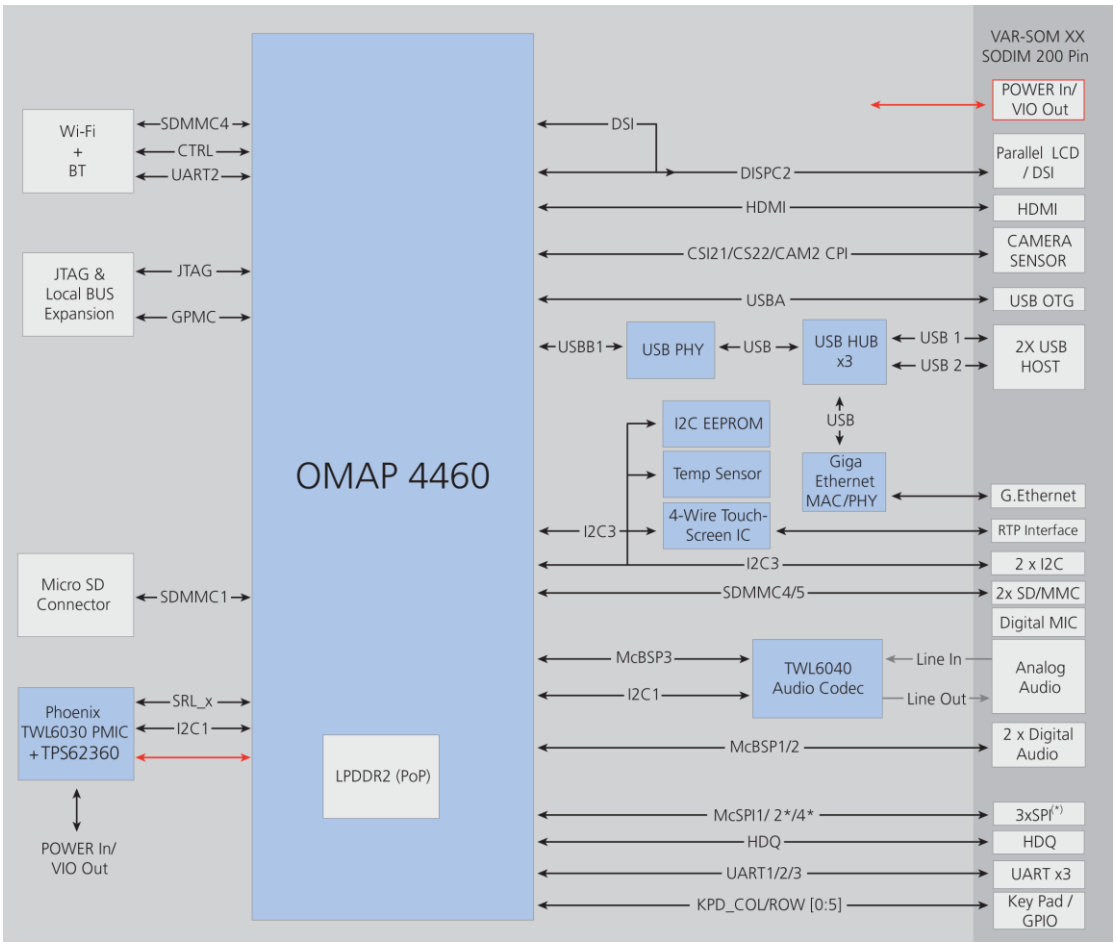
- VAR-OM44CustomBoard – evaluation board
  - ✓ Carrier -Board, compatible with VAR-SOM-OM44
  - ✓ Schematics
- O.S support
  - ✓ Android
  - ✓ Linux

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2 Feature Summary

- Texas Instruments OMAP4460 CPU:
  - Up to 1.5 GHz Dual Core ARM Cortex™-A9 Processor with 1MB L2 cache. Each core has:
    - NEON™ Advanced SIMD and Vector Floating Point Unit (VFPv3) coprocessors
    - 32 KB Instruction an 32 KB Data L1 cache
  - High Definition image and video hardware accelerator (IVA-HD 1.0)
  - PowerVR™ SGX540 2D/3D graphics accelerator
  - DSP sub-system based on TMS320DMC64x+™ very long instruction word (VLIW) DSP core with 32 KB L1 cache and 128 KB L2 cache running at
- 512-1024 MB LPDDR2 SDRAM
- Micro SD socket for storage and boot
- Gigabit Ethernet controller & PHY
- WLAN 802.11 b/g/n
- Dual Display:
  - 24-bit Parallel RGB
  - HDMI
  - Serial Display Interface (DSI)
- Resistive touch screen interface (4wire)
- RAW image-sensor module interface
  - 16-bit Camera Parallel Interface (CPI)
  - 2 x Camera Serial Interface (CSI2)
- USB:
  - 2 x USB 2.0 high-speed host interface
  - USB 2.0 OTG interface
- Audio:
  - Head phone-out
  - Line-in
  - S/PDIF out
  - Digital microphone interface
  - Multichannel buffered serial port
- 2 x SDIO/MMC interface
- Local BUS (GPMC) Interface
- Bluetooth
- Keypad interface
- UART ports
- SPI
- I2C interfaces
- 1 – wire/ HDQ
- JTAG
- On board temperature sensor
- Power:
  - Single 3.3 V DC-IN power supply
  - RTC back-up battery input

1.3 Block Diagram



2 Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-OM44

2.1 Texas Instruments OMAP4460

2.1.1 Overview

The OMAP4460 high-performance applications processor is based on the enhanced OMAP™ 4 architecture and uses 45 nm process technology.

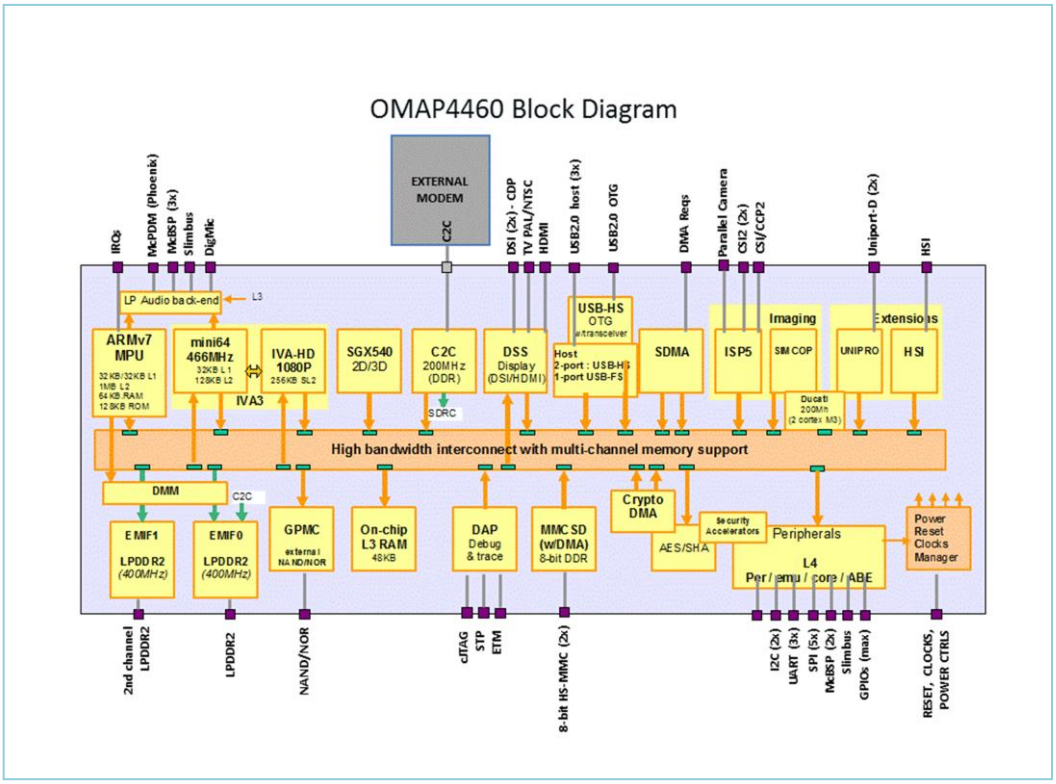
The architecture is designed to provide best-in-class video, image and graphics processing which can support the following:

- Streaming video up to full HD
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still image
- Video capture

The following subsystems are part of the OMPA4460 device:

- Up to 1.5 GHz , ARM® Cortex™-A9 microprocessor unit (MPU) subsystem based on the microprocessor, including two ARM® Cortex-A9 cores
- Digital Signal Processor (DSP) subsystem
- Image and Video Accelerator High-Definition (IVA-HD) subsystem
- Cortex™-M3 MPU subsystem, including two ARM Cortex-M3 microprocessors
- Display subsystem
- Audio Back-End (ABE) subsystem
- Imaging Sub-System (ISS), consisting of Image Signal Processor (ISP) and Still Image CO-Processor (SIMCOP) block
- 2D/3D graphic accelerator (SGX) subsystem
- Emulation (EMU) subsystem

2.1.2 OMAP4460 Block Diagram



2.1.3 MPU Subsystem

The MPU subsystem integrates the following modules:

The Cortex-A9 MPU subsystem, integrating the following sub-modules:

- ARM Cortex-A9 MPCore
  - Two ARM Cortex-A9 central processing units (CPUs)
  - ARM Version 7 ISA™: Standard ARM instruction set plus Thumb®-2, Jazelle® RCT and Jazelle DBX Java™ accelerators
  - Neon™ SIMD coprocessor and VFPv3 per CPU
  - Interrupt controller (Cortex-A9 MPU INTC) with up to 128 interrupt requests
  - One general-purpose timer and one watchdog timer per CPU
  - Debug and trace features
  - 32 KB instruction and 32 KB data level 1 (L1) caches per CPU
- Shared 1 MB level 2 (L2) cache
- 48 KB bootable ROM
- Local power, reset, and clock management (PRCM) module
- Emulation features
- Digital phase-locked loop (DPLL)

2.1.4 External Memory Interfaces

The OMAP™ 4 includes two external memory interfaces:

- General Purpose Memory Controller (GPMC): The GPMC is an unified memory controller dedicated to interfacing external memory devices:

  - Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
  - Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
  - NAND Flash
  - Pseudo-SRAM devices
- EMIF Module: The EMIF module provides connectivity between the device and the LPDDR2-type memories and manages data bus read/write accesses between external memories, the microprocessor unit (MPU) and the direct memory access (DMA) controller.

2.1.5 DMA Controllers

The device embeds one generic DMA controller, the system DMA (sDMA) controller, used for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers:

- One read port, one write port
- 32 logical DMA channels supporting among other features:
  - 8-bit, 16-bit, or 32-bit data element transfer size
  - Software-triggered or hardware-synchronized transfers
  - Flexible source and destination address generation
  - Burst read and write
  - Chained multiple-channel transfers
  - Endianism conversion
  - Draining
- Up to 127 DMA requests
- 256 x 64-bit FIFO dynamically allocable between active channels

2.1.6 Display Subsystem

The Display Sub-System (DSS) provides the logic to display a video frame from the memory frame buffer on a Liquid Crystal Display (LCD) panel or a TV set.

LCD Interface:

The primary LCD output:
- DSI1 (MIPI® DSI) - SXGA (1400x1050) VESA timing @ 60 FPS

The secondary LCD output:
- Parallel RGB output (MIPI DPI 1.0) - SXGA (1400x1050) VESA timing @ 85 fps1080i/720p

HDMI interface:
High-Definition Multimedia Interface (using TV set out) - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI

2.1.7 IVA-HD Subsystem

The IVA-HD subsystem is a set of video encoder/decoder hardware accelerators. It supports up to 1080p × 30 fps, slow-motion camcorder, triple play (HD and SD capture

and JPEG capture), real-time transcoding of up to 720p, and video conferencing up to 720p.

The IVA-HD supports the following formats:

- MPEG-1/-2/-4 such as MPEG-2 MP, ML, and MPEG-4 as SP/ASP
- DivX 5.02 and above
- Sorenson Spark (decode)
- H.263 P0 (encode/decode) and P3 (decode)
- H.264 Annex G (scalable baseline profile up to 720p)
- H.264 BL/MP/HP
- H.264 Annex H (partial)
- Stereoscopic video
- JPEG (encode/decode)
- VC-1 SP/MP/AP
- AVS-1.0
- RealVideo® 8/9/10 (decode only)
- On2® VP6.2/VP7 (decode only)

2.1.8 2D and 3D Graphics Accelerator (SGX)

The 2D/3D graphics accelerator (SGX) subsystem accelerates 2-Dimensional (2D) and 3-Dimensional (3D) graphics applications. The SGX subsystem is based on the PowerVR® SGX core from Imagination Technologies. SGX is a new generation of programmable PowerVR graphics IP cores. The PowerVR SGX540 v1.2.0 architecture is scalable and can target all market segments from mainstream mobile devices to high-end desktop graphics. PowerVR® SGX main features:

- 3D graphics, vector graphics, and video supported on common hardware
- Tile-based architecture
- Universal Scalable Shader Engine (USSE™): a multi-threaded engine that incorporates pixel and vertex shader functionality and reduces die area
- Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OpenGL™2.0
- Industry standard application programming interface (API) support: OpenGL ES 1.1 and 2.0, OpenVG v1.1
- Fine-grained task switching, load balancing, and power management
- Advanced geometry, direct memory access (DMA)-driven operation for minimum CPU interaction
- Programmable high-quality image anti-aliasing
- Fully virtualized memory addressing for Operating System (OS) functioning in a unified memory architecture

2.1.9 Imaging Sub-System

The Imaging Sub-System (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory (image format encoding and decoding can be done to and from memory), or data from SL2 in IVA-HD for hardware encoding. With subparts, such as interfaces and interconnects, Image Signal Processor (ISP), and Still

Image COProcessor (SIMCOP), the ISS is a key component for the following multimedia applications: Camera viewfinder, video record, and still image capture.

The ISS is mainly composed of CCP2 and CSI2-A, CSI2-B camera interfaces, a parallel interface (CPI), an ISP and a block-based imaging accelerator (SIMCOP). The ISS is designed to reach high throughput and low latency with large image sensors. In high-performance mode, the ISS supports a pixel throughput of 200 MPix/s.

The ISS targets the following major use cases:

- Viewfinder with digital zoom, video stabilization, and rotations
- Up to 1080 p video record at 30 fps with digital zoom, video stabilization, and rotation
  Up to 16 MPix still image capture with digital zoom and rotation
  High performance mode: Up to 200 MPix/s throughput
- High quality and low light modes: Up to 50 MPix/s throughputs
- Still image capture during video record

2.1.10 Audio Back End

The Audio Back End (ABE) module is a subsystem that manages various audio and voice uplink and downlink streams between the initiator (the Cortex™-A9 microprocessor unit [MPU], Digital Signal Processor [DSP], or Direct Memory Access [DMA] controller) and the peripheral physical interfaces (Multichannel Buffered Serial Port [McBSP], SLIMbus®, Digital MICrocontroller [DMIC], Multichannel Pulse Density Modulation [McPDM], and Multichannel Audio Serial Port [McASP]). In addition it contains Audio Engine (AE) that performs some real-time signal processing like sample rate conversion, filtering, equalizing, and side-tone.

2.2 Memory

2.2.1 RAM

The VAR-SOM-OM44 is available with 512 or 1024 MB of LPDDR2 memory, using Package-on-Package (PoP) technology.

2.2.2 Non-volatile Storage Memory

The on board micro-SD connector is used for boot and as a mass storage device.

2.2.3 I2C EEPROM

8K EEPROM device is used for storing boot arguments, Giga Ethernet MAC address and other propriety data.

2.3 LAN7500 10/100/1000 Gigabit Ethernet Controller

SMSC's LAN7500 is a Hi-Speed USB 2.0 to 10/100/1000 Gigabit Ethernet controller providing a high-performance Ethernet connectivity solution. The LAN7500 contains an integrated 10/100/1000 Gigabit Ethernet PHY, USB PHY, Hi-Speed USB 2.0 device controller, 10/100/1000 Gigabit Ethernet MAC, TAP controller, EEPROM controller and a FIFO controller with a total of 32 KB internal packet buffering. The device supports 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet and implements control, interrupt, Bulk-IN and Bulk-OUT USB endpoints. The Ethernet controller supports auto-negotiation,

auto-polarity correction, HP Auto-MDIX support and is compliant with IEEE 802.3/802.3u/802.3ab standards.

2.4 TWL6040 Audio

The TWL6040 device is an audio coder/decoder (codec) with a high level of integration providing analog audio codec functions for portable applications. It contains multiple audio analog inputs and outputs, as well as microphone biases and accessory detection. The device is connected to the OMAP4™ host processor through a proprietary PDM interface for audio data communication enabling partitioning with optimized power consumption and performance. Multichannel audio data is multiplexed to a single wire for downlink (PDML) and uplink (PDMUL).

VAR-SOM-OM44 utilizes TWL6040's line-in and the headphone driver analog interfaces.

2.5 TWL6030 PMIC

The TWL6030 is a dedicated integrated power-management IC for the OMAP4™ platform and supports the OMAP4460 power-management architecture to ensure maximum performance and operation time for user satisfaction (audio/video support) while offering versatile power-management techniques for maximum design flexibility, depending on application requirements.

The device provides seven configurable step-down converters with up to 1.6 A capability for memory, processor core, I/O, auxiliary, pre-regulation for LDOs, etc. The device also contains 11 LDO regulators that can be supplied from a battery or a pre-regulated supply. Power-up/power-down controller is configurable and can support any power-up/power-down sequences (EPROM based). The Real-Time Clock (RTC) provides a 32-kHz output buffer, second/minute/hour/day/ month/year information and alarm wake up.

3 External Connectors

The VAR-SOM-OM44 exposes a 200 pin SO–DIMM mechanical standard interface. The recommended mating connector for baseboard interfacing is FCI 10033853-052FSLF or equivalent. An additional 40 pin FPC expansion connector exposes the GPMC and JTAG interfaces of the OMAP4460 SoC an example for a mating cable is Molex 21020-0427.

The following list describes this chapter's column header tables:

Pin#:
Pin Number on the SO-DIMM200 connector (excluding GPMC & JTAG interfaces which are exposed by the 40-pin FCC connector)

Pin Name:
Default VAR-OM44 Pin Name

Type:
Pin Type & Direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin Functionality group

OMAP4 Ball:
OMAP4460 ball number

Mode (Tables 3.2 & 3.4):
OMAP4™ – Pin Mux mode option

3.1 SoM Connector Pin Out

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
1	DGND	POWER	Digital GND	
2	DGND	POWER	Digital GND	
3	DISPC2_DATA3	IO	DPI / Pin Mux Table 3.2	AB2
4	DISPC2_DATA2	IO	DPI / Pin Mux Table 3.2	AB3
5	DISPC2_DATA5	IO	DPI / Pin Mux Table 3.2	AA3
6	DISPC2_DATA4	IO	DPI / Pin Mux Table 3.2	AA4
7	DISPC2_DATA7	IO	DPI / Pin Mux Table 3.2	AA1
8	DISPC2_DATA6	IO	DPI / Pin Mux Table 3.2	AA2

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
9	DGND	POWER	Digital GND	
10	DGND	POWER	Digital GND	
11	DISPC2_DATA11	IO	DPI / Pin Mux Table 3.2	AE9
12	DISPC2_DATA10	IO	DPI / Pin Mux Table 3.2	V1
13	DISPC2_DATA13	IO	DPI / Pin Mux Table 3.2	AF10
14	DISPC2_DATA12	IO	DPI / Pin Mux Table 3.2	AG10
15	DISPC2_DATA15	IO	DPI / Pin Mux Table 3.2	AH11
16	DISPC2_DATA14	IO	DPI / Pin Mux Table 3.2	AE10
17	DISPC2_DATA17	IO	DPI / Pin Mux Table 3.2	W2
18	DGND	POWER	Digital GND	
19	DISPC2_DATA19	IO	DPI / Pin Mux Table 3.2	AF11
20	DISPC2_DATA18	IO	DPI / Pin Mux Table 3.2	AG11
21	DISPC2_DATA21	IO	DPI / Pin Mux Table 3.2	AG13
22	DISPC2_DATA20	IO	DPI / Pin Mux Table 3.2	AE11
23	DISPC2_DATA23	IO	DPI / Pin Mux Table 3.2	AF12
24	DISPC2_DATA22	IO	DPI / Pin Mux Table 3.2	AE12
25	DGND	POWER	Digital GND	
26	DISPC2_HSYNC	IO	DPI / Pin Mux Table 3.2	W3
27	MCBSP1_CLKX	IO	MCBSP1 Interface / Pin Mux Table 3.2	AC26
28	DISPC2_PCLK	IO	DPI / Pin Mux Table 3.2	W4
29	UART3_CTS_RCTX	IO	UART3 Port / Pin Mux Table 3.2	F27
30	DGND	POWER	Digital GND	
31	UART3_RTS_IRSD	IO	UART3 Port / Pin Mux Table 3.2	F28
32	SDMMC2_CLK	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AE5
33	UART3_RX_IRRX	IO	UART3 Port / Pin Mux Table 3.2	G27
34	MCSPI1_CS0	IO	SPI1 Interface / Pin Mux Table 3.2	AE23
35	UART3_TX_IRTX	IO	UART3 Port / Pin Mux Table 3.2	G28
36	SDMMC2_DAT0	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AE4
37	MCSPI1_CLK	IO	SPI1 Interface / Pin Mux Table 3.2	AF22
38	SDMMC2_DAT1	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AF4
39	MCSPI1_SIMO	IO	SPI1 Interface / Pin Mux Table 3.2	AG22
40	SDMMC2_DAT2	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AG3
41	MCSPI1_SOMI	IO	SPI1 Interface / Pin Mux Table 3.2	AE22
42	SDMMC2_DAT3	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AF3
43	SDMMC2_CMD	IO	MMC/SD/SDIO2 / Pin Mux Table 3.2	AF5

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
44	NC			
45	DISPC2_DATA16	IO	DPI / Pin Mux Table 3.2	W1
46	DISPC2_VSYNC	IO	DPI / Pin Mux Table 3.2	Y2
47	DGND	POWER	Digital GND	
48	DGND	POWER	Digital GND	
49	FREF_CLK1_OUT	IO	Reference Clock Out / Pin Mux Table 3.2	AA28
50	CSI21_DX0	I	Camera Interface / Pin Mux Table 3.2	R26
51	DGND	POWER	Digital GND	
52	CSI21_DY0	I	Camera Interface / Pin Mux Table 3.2	R25
53	CSI21_DX3	I	Camera Interface / Pin Mux Table 3.2	V26
54	CSI21_DY2	I	Camera Interface / Pin Mux Table 3.2	U25
55	CSI21_DY3	I	Camera Interface / Pin Mux Table 3.2	V25
56	CSI21_DX2	I	Camera Interface / Pin Mux Table 3.2	U26
57	DGND	POWER	Digital GND	
58	DGND	POWER	Digital GND	
59	CAM_GLB_RESET	IO	Camera Interface / Pin Mux Table 3.2	V27
60	DGND	POWER	Digital GND	
61	I2C3_SDA	IO	I2C3 Interface[1]	Y27
62	DISPC2_DATA9	IO	DPI / Pin Mux Table 3.2	V2
63	I2C3_SCL	IO	I2C3 Interface[1]	W27
64	DISPC2_DE	IO	DPI / Pin Mux Table 3.2	Y3
65	UART2_CTS	IO	UART2 Port/ / Pin Mux Table 3.2 [2]	AB26
66	DISPC2_DATA0	IO	DPI / Pin Mux Table 3.2	AC4
67	UART2_RTS	IO	UART2 Port/ / Pin Mux Table 3.2 [2]	AB27
68	DISPC2_DATA1	IO	DPI / Pin Mux Table 3.2	AB4
69	UART2_TX	IO	UART2 Port/ / Pin Mux Table 3.2 [2]	AA26
70	DISPC2_DATA8	IO	DPI / Pin Mux Table 3.2	Y4
71	UART2_RX	IO	UART2 Port/ / Pin Mux Table 3.2 [2]	AA25
72	CAM_SHUTTER	IO	Camera Interface / Pin Mux Table 3.2	T27
73	TSPX	A	Resistive Touch Screen Interface	
74	DGND	POWER	Digital GND	
75	TSPY	A	Resistive Touch Screen Interface	
76	KPD_ROW1	IO	Keypad Interface / Pin Mux Table 3.2	L27
77	TSMX	A	Resistive Touch Screen Interface	

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
78	KPD_ROW0	IO	Keypad Interface / Pin Mux Table 3.2	K25
79	TSMY	A	Resistive Touch Screen Interface	
80	CAM_STROBE	IO	Camera Interface / Pin Mux Table 3.2	U27
81	DGND	POWER	Digital GND	
82	HDQ_SIO	IO	One Wire Interface / Pin Mux Table 3.2	AA27
83	DGND	POWER	Digital GND	
84	UART1_TX	IO	UART1 Port / Pin Mux Table 3.2	D26
85	KPD_ROW3	IO	Keypad Interface / Pin Mux Table 3.2	J26
86	UART1_RTS	IO	UART1 Port / Pin Mux Table 3.2	AH23
87	KPD_ROW2	IO	Keypad Interface / Pin Mux Table 3.2	K27
88	UART1_CTS	IO	UART1 Port / Pin Mux Table 3.2	AG23
89	NC			
90	UART1_RX	IO	UART1 Port / Pin Mux Table 3.2	C26
91	NC			
92	BOOTSEL	IO	Boot Source Select – NC for Internal Boot / Logic ‘1’ for MMC/SD/SDIO2 Boot	
93	MCBSP1_FSX	IO	MCBSP1 Interface / Pin Mux Table 3.2	AC27
94	DGND	POWER	Digital GND	
95	MCBSP1_DX	IO	MCBSP1 Interface / Pin Mux Table 3.2	AB25
96	DGND	POWER	Digital GND	
97	GPIO_13	IO	GPIO 13 / Pin Mux Table 3.2	P2
98	MCBSP2_CLKX	IO	MCBSP2 Interface / Pin Mux Table 3.2	AD27
99	I2C4_SDA	IO	I2C4 Interface / Pin Mux Table 3.2	AH22
100	VBAT_SOM	POWER	Main Power	
101	I2C4_SCL	IO	I2C4 Interface / Pin Mux Table 3.2	AG21
102	MCBSP2_DR	IO	MCBSP2 Interface / Pin Mux Table 3.2	AD26
103	USBH_DP1	IO	USB HOST1	
104	MCBSP2_DX	IO	MCBSP2 Interface / Pin Mux Table 3.2	AD25
105	USBH_DN1	IO	USB HOST1	
106	MCBSP2_FSX	IO	MCBSP2 Interface / Pin Mux Table 3.2	AC28
107	USB_HOST1_OC	I	USB Host1 Over Current	
108	VBAT_SOM	POWER	Main Power	
109	NC			

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
110	VBAT_SOM	POWER	Main Power	
111	USB_HOST2_OC	I	USB Host2 Over Current	
112	VBAT_SOM	POWER	Main Power	
113	VBAT_SOM	POWER	Main Power	
114	VBAT_SOM	POWER	Main Power	
115	VBAT_SOM	POWER	Main Power	
116	VBAT_SOM	POWER	Main Power	
117	VIO	POWER	Main Power	
118	USBOTG_VBUS	POWER	USB OTG Bus Power	
119	DGND	POWER	Digital GND	
120	USB_OTG_DP	IO	USB On The Go / Pin Mux Table 3.2	B5
121	USBH_DP2	IO	USB HOST2	
122	USB_OTG_DM	IO	USB On The Go / Pin Mux Table 3.2	B4
123	USBH_DN2	IO	USB HOST2	
124	USB_OTG_ID	I	USB On The Go Device Type	
125	DGND	POWER	Digital GND	
126	RTC_BAT	POWER	Real-Time Clock Power In	
127	RESET_IN_N	I	Reset In - Active Low	
128	DGND	POWER	Digital GND	
129	CSI21_DX4	I	Camera Interface / Pin Mux Table 3.2	W26
130	CSI21_DX1	I	Camera Interface / Pin Mux Table 3.2	T26
131	CSI21_DY4	I	Camera Interface / Pin Mux Table 3.2	W25
132	CSI21_DY1	I	Camera Interface / Pin Mux Table 3.2	T25
133	DGND	POWER	Digital GND	
134	DGND	POWER	Digital GND	
135	CSI22_DX1	I	Camera Interface / Pin Mux Table 3.2	N26
136	CSI22_DY2	I	Camera Interface / Pin Mux Table 3.2	M27
137	CSI22_DY1	I	Camera Interface / Pin Mux Table 3.2	N25
138	CSI22_DX2	I	Camera Interface / Pin Mux Table 3.2	N27
139	DGND	POWER	Digital GND	
140	DGND	POWER	Digital GND	
141	CSI22_DX0	ODS	Camera Interface / Pin Mux Table 3.2	M26
142	HDMI_DATA1X	A	HDMI Interface	C9

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
143	CSI22_DY0	I	Camera Interface / Pin Mux Table 3.2	M25
144	HDMI_DATA1Y	ODS	HDMI Interface	D9
145	DGND	POWER	Digital GND	
146	DGND	POWER	Digital GND	
147	HDMI_DATA0Y	ODS	HDMI Interface	D10
148	HDMI_CLOCKY	ODS	HDMI Interface	D11
149	HDMI_DATA0X	ODS	HDMI Interface	C10
150	HDMI_CLOCKX	ODS	HDMI Interface	C11
151	DGND	POWER	Digital GND	
152	HDMI_CEC	IO	Consumer Electronic Control / Pin Mux Table 3.2	B10
153	HDMI_DDC_SDA	IO	HDMI Display Data Control / Pin Mux Table 3.2	B8
154	HDMI_DDC_SCL	IO	HDMI Display Data Control / Pin Mux Table 3.2	A8
155	HDMI_DATA2X	A	HDMI Interface	C8
156	DGND	POWER	Digital GND	
157	HDMI_DATA2Y	A	HDMI Interface	D8
158	PWM0	IO	PWM / Pin Mux Table 3.2	AH24
159	DGND	POWER	Digital GND	
160	HDMI_HPD	IO	HDMI Hotplug detect / Pin Mux Table 3.2	B9
161	LINK_LED	O	Ethernet Link Indication	
162	DGND	POWER	Digital GND	
163	SPEED_LED	O	Ethernet Speed Indication	
164	SDMMC4_CLK	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AE21
165	GETH_TXN	IODS	Ethernet Interface	
166	SDMMC4_CMD	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AF20
167	GETH_TXP	IODS	Ethernet Interface	
168	SDMMC4_DAT0	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AF21
169	DGND	POWER	Digital GND	
170	SDMMC4_DAT1	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AH19
171	GETH_RXN	IODS	Ethernet Interface	
172	SDMMC4_DAT2	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AG20
173	GETH_RXP	IODS	Ethernet Interface	
174	SDMMC4_DAT3	IO	MMC/SD/SDIO4 / Pin Mux Table 3.2[3]	AE20
175	DGND	POWER	Digital GND	

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
176	MCBSP1_DR	IO	MCBSP1 Interface / Pin Mux Table 3.2	AC25
177	GETH_D2N	IODS	Ethernet Interface	
178	DGND	POWER	Digital GND	
179	GETH_D2P	IODS	Ethernet Interface	
180	KPD_COL5	IO	Keypad Interface / Pin Mux Table 3.2	H26
181	DGND	POWER	Digital GND	
182	KPD_COL4	IO	Keypad Interface / Pin Mux Table 3.2	G25
183	GETH_D3N	IODS	Ethernet Interface	
184	DGND	POWER	Digital GND	
185	GETH_D3P	IODS	Ethernet Interface	ETH IC
186	DMIC_CLK	IO	Digital Microphone Clock / Pin Mux Table 3.2	AE24
187	DGND	POWER	Digital GND	
188	DMIC_DATA	IO	Digital Microphone Data /Pin Mux Table 3.2	AG24
189	KPD_COL3	IO	Keypad Interface / Pin Mux Table 3.2	G26
190	DGND	POWER	Digital GND	
191	KPD_COL2	IO	Keypad Interface / Pin Mux Table 3.2	H27
192	KPD_COL0	IO	Keypad Interface / Pin Mux Table 3.2	H25
193	NC			
194	KPD_COL1	IO	Keypad Interface / Pin Mux Table 3.2	J27
195	AGND	POWER	Audio GND	
196	AGND	POWER	Audio GND	
197	AUDIO_IN_L	A	Audio Line In Left	
198	HP_OUT_L	A	Headphone Out Left	
199	AUDIO_IN_R	A	Audio Line In Right	
200	HP_OUT_R	A	Headphone Out Right	

Table 3-1 SO-DIMM200 Pin Out

Notes:

[1] The I2C3 Interface is used on board. Pin mode can't be changed.

[2] The UART2 is used for on board Bluetooth connectivity. Pin mode can't be changed if Bluetooth is enabled.

[3] The MMC/SD/SDIO4 is used for on board Wi-Fi connectivity. Pin mode can't be changed if Wi-Fi is enabled.

3.2 SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each SO-DIMM 200 connector. Default pin mode is marked in bold.

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
3	DPM_EMU16	DMTIMER8_PWM_EVT	DSI1_TE0	GPIO_27	RFBI_DATA3	**DISPC2_DATA3**
4	DPM_EMU17	DMTIMER9_PWM_EVT	DSI1_TE1	GPIO_28	RFBI_DATA2	**DISPC2_DATA2**
5	DPM_EMU14	SYS_DRM_MSECURE	UART1_RX	GPIO_25	RFBI_DATA5	**DISPC2_DATA5**
6	DPM_EMU15	SYS_SECURE_INDICATOR		GPIO_26	RFBI_DATA4	**DISPC2_DATA4**
7	DPM_EMU12	USBA0_ULPIPHY_DAT6		GPIO_23	RFBI_DATA7	**DISPC2_DATA7**
8	DPM_EMU13	USBA0_ULPIPHY_DAT7		GPIO_24	RFBI_DATA6	**DISPC2_DATA6**
11	USBB2_ULPITLL_DAT7	USBB2_ULPIPHY_DAT7	SDMMC3_CLK	GPIO_168	MCSPI3_CLK	**DISPC2_DATA11**
12	DPM_EMU3	USBA0_ULPIPHY_STP		GPIO_14	RFBI_DATA10	**DISPC2_DATA10**
13	USBB2_ULPITLL_DAT5	USBB2_ULPIPHY_DAT5	SDMMC3_DAT3	GPIO_166	MCSPI3_CS0	**DISPC2_DATA13**
14	USBB2_ULPITLL_DAT6	USBB2_ULPIPHY_DAT6	SDMMC3_CMD	GPIO_167	MCSPI3_SIMO	**DISPC2_DATA12**
15	USBB2_ULPITLL_DAT3	USBB2_ULPIPHY_DAT3	SDMMC3_DAT1	GPIO_164	HSI2_CAREADY	**DISPC2_DATA15**
16	USBB2_ULPITLL_DAT4	USBB2_ULPIPHY_DAT4	SDMMC3_DAT0	GPIO_165	MCSPI3_SOMI	**DISPC2_DATA14**
17	DPM_EMU6	USBA0_ULPIPHY_DAT0	UART3_TX_IRTX	GPIO_17	RFBI_HSYNC0	**DISPC2_DATA17**
19	USBB2_ULPITLL_DAT1	USBB2_ULPIPHY_DAT1	SDMMC4_DAT3	GPIO_162	HSI2_ACDATA	**DISPC2_DATA19**
20	USBB2_ULPITLL_DAT2	USBB2_ULPIPHY_DAT2	SDMMC3_DAT2	GPIO_163	HSI2_ACFLAG	**DISPC2_DATA18**
21	USBB2_ULPITLL_NXT	USBB2_ULPIPHY_NXT	SDMMC4_DAT1	GPIO_160	HSI2_ACREADY	**DISPC2_DATA21**
22	USBB2_ULPITLL_DAT0	USBB2_ULPIPHY_DAT0	SDMMC4_DAT2	GPIO_161	HSI2_ACWAKE	**DISPC2_DATA20**
23	USBB2_ULPITLL_STP	USBB2_ULPIPHY_STP	SDMMC4_CLK	GPIO_158	HSI2_CADATA	**DISPC2_DATA23**
24	USBB2_ULPITLL_DIR	USBB2_ULPIPHY_DIR	SDMMC4_DAT0	GPIO_159	HSI2_CAFLAG	**DISPC2_DATA22**
26	DPM_EMU7	USBA0_ULPIPHY_DAT1	UART3_RX_IRRX	GPIO_18	RFBI_CS0	**DISPC2_HSYNC**
27	**ABE_MCBSP1_CLKX**	ABE_SLIMBUS1_CLOCK		GPIO_114		
28	DPM_EMU8	USBA0_ULPIPHY_DAT2	UART3_RTS_SD	GPIO_19	RFBI_RE	**DISPC2_PCLK**
29	**UART3_CTS_RCTX**	UART1_TX		GPIO_141		
31	**UART3_RTS_SD**		CAM_GLOBALRESET	GPIO_142		
32	SDMMC5_CLK	MCSPI2_CLK	USBC1_ICUSB_DP	GPIO_145		**SDMMC2_CLK**
33	**UART3_RX_IRRX**	DMTIMER8_PWM_EVT		GPIO_143		
34	**MCSPI1_CS0**			GPIO_137		
35	**UART3_TX_IRTX**	DMTIMER9_PWM_EVT	CAM_STROBE	GPIO_144		
36	SDMMC5_DAT0	MCSPI2_SOMI	USBC1_ICUSB_RCV	GPIO_147		**SDMMC2_DAT0**
37	**MCSPI1_CLK**			GPIO_134		
38	SDMMC5_DAT1		USBC1_ICUSB_TXEN	GPIO_148		**SDMMC2_DAT1**
39	MCSPI1_SIMO			GPIO_136		
40	SDMMC5_DAT2	MCSPI2_CS1		GPIO_149		**SDMMC2_DAT2**
41	**MCSPI1_SOMI**			GPIO_135		
42	SDMMC5_DAT3	MCSPI2_CS0		GPIO_150		**SDMMC2_DAT3**
43	SDMMC5_CMD	MCSPI2_SIMO	USBC1_ICUSB_DM	GPIO_146		**SDMMC2_CMD**
45	DPM_EMU5	USBA0_ULPIPHY_NXT		GPIO_16	RFBI_TE_VSYNC0	**DISPC2_DATA16**
46	DPM_EMU9	USBA0_ULPIPHY_DAT3	UART3_CTS_RCTX	GPIO_20	RFBI_WE	**DISPC2_VSYNC**
49	**FREF_CLK1_OUT**			GPIO_181		
50	**CSI21_DX0**			GPI_67		
52	**CSI21_DY0**			GPI_68		
53	**CSI21_DX3**	CAM2_D7		GPI_73		
54	**CSI21_DY2**			GPI_72		
55	**CSI21_DY3**	CAM2_D6		GPI_74		
56	**CSI21_DX2**			GPI_71		
59	**CAM_GLOBALRESET**		CAM2_PCLK	GPIO_83		
62	DPM_EMU4	USBA0_ULPIPHY_DIR		GPIO_15	RFBI_DATA9	**DISPC2_DATA9**
64	DPM_EMU10	USBA0_ULPIPHY_DAT4		GPIO_21	RFBI_A0	**DISPC2_DE**
65	**UART2_CTS**	SDMMC3_CLK		GPIO_123		
66	DPM_EMU19	DMTIMER11_PWM_EVT	DSI2_TE1	GPIO_191	RFBI_DATA0	**DISPC2_DATA0**
67	**UART2_RTS**	SDMMC3_CMD		GPIO_124		
68	DPM_EMU18	DMTIMER10_PWM_EVT	DSI2_TE0	GPIO_190	RFBI_DATA1	**DISPC2_DATA1**
69	**UART2_TX**	SDMMC3_DAT1		GPIO_126		
70	DPM_EMU11	USBA0_ULPIPHY_DAT5		GPIO_22	RFBI_DATA8	**DISPC2_DATA8**

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
71	**UART2_RX**	SDMMC3_DAT0		GPIO_125		
72	**CAM_SHUTTER**		CAM2_HS	GPIO_81		
76	**KPD_ROW1**	KPD_ROW4	CAM2_D9	GPIO_2		
78	**KPD_ROW0**	KPD_ROW3	CAM2_D7	GPIO_178		
80	**CAM_STROBE**		CAM2_VS	GPIO_82		
82	**HDQ_SIO**	I2C3_SCCB	I2C2_SCCB	GPIO_127		
84	**I2C2_SDA**	UART1_TX		GPIO_129		
85	**KPD_ROW3**	KPD_ROW0	CAM2_D4	GPIO_175		
86	MCSPI1_CS3	**UART1_RTS**	SLIMBUS2_DATA	GPIO_140		
87	**KPD_ROW2**	KPD_ROW5	CAM2_D11	GPIO_3		
88	MCSPI1_CS2	**UART1_CTS**	SLIMBUS2_CLOCK	GPIO_139		
90	I2C2_SCL	**UART1_RX**		GPIO_128		
93	**ABE_MCBSP1_FSX**	SDMMC3_DAT3	ABE_MCASP_AMUTEIN	GPIO_117		
95	**ABE_MCBSP1_DX**	SDMMC3_DAT2	ABE_MCASP_ACLKX	GPIO_116		
97	DPM_EMU2	USBA0_ULPIPHY_CLK		**GPIO_13**		DISPC2_FID
98	**ABE_MCBSP2_CLKX**	MCSPI2_CLK	ABE_MCASP_AHCLKX	GPIO_110	USBB2_MM_RXDM	
99	**I2C4_SDA**			GPIO_133		
101	**I2C4_SCL**			GPIO_132		
102	**ABE_MCBSP2_DR**	MCSPI2_SOMI	ABE_MCASP_AXR	GPIO_111	USBB2_MM_RXDP	
104	**ABE_MCBSP2_DX**	MCSPI2_SIMO	ABE_MCASP_AMUTE	GPIO_112	USBB2_MM_RXRCV	
106	**ABE_MCBSP2_FSX**	MCSPI2_CS0	ABE_MCASP_AFSX	GPIO_113	USBB2_MM_TXEN	
120	**USBA0_OTG_DP**	UART3_RX_IRRX	UART2_RX			
122	**USBA0_OTG_DM**	UART3_TX_IRTX	UART2_TX			
129	**CSI21_DX4**	CAM2_D5		GPI_75		
130	**CSI21_DX1**			GPI_69		
131	**CSI21_DY4**	CAM2_D4		GPI_76		
132	**CSI21_DY1**			GPI_70		
135	**CSI22_DX1**	CAM2_D1	CAM_D14	GPI_79		
136	**CSI22_DY2**		CAM2_WEN			
137	**CSI22_DY1**	CAM2_D0	CAM_D15	GPI_80		
138	**CSI22_DX2**		CAM2_FLD			
141	**CSI22_DX0**	CAM2_D3	CAM_D12	GPI_77		
143	**CSI22_DY0**	CAM2_D2	CAM_D13	GPI_78		
152	**HDMI_CEC**			GPIO_64		
153	**HDMI_DDC_SDA**			GPIO_66		
154	**HDMI_DDC_SCL**			GPIO_65		
158	ABE_DMIC_DIN3	SLIMBUS2_DATA	ABE_DMIC_CLK2	GPIO_122		**DMTIMER9_PWM_EVT**
160	**HDMI_HPD**			GPIO_63		
164	**MCSPI4_CLK**	SDMMC4_CLK	KPD_COL6	GPIO_151		
166	**MCSPI4_SIMO**	SDMMC4_CMD	KPD_COL7	GPIO_152		
168	**MCSPI4_SOMI**	SDMMC4_DAT0	KPD_ROW6	GPIO_153		
170	**UART4_TX**	SDMMC4_DAT1	KPD_COL8	GPIO_156		
172	**UART4_RX**	SDMMC4_DAT2	KPD_ROW8	GPIO_155		
174	**MCSPI4_CS0**	SDMMC4_DAT3	KPD_ROW7	GPIO_154		
176	**ABE_MCBSP1_DR**	ABE_SLIMBUS1_DATA		GPIO_115		
180	**KPD_COL5**	KPD_COL2	CAM2_D2	GPIO_173		
182	**KPD_COL4**	KPD_COL1	CAM2_D1	GPIO_172		
186	**ABE_DMIC_CLK1**			GPIO_119	USBB2_MM_TXSE0	UART4_CTS
188	**ABE_DMIC_DIN2**	SLIMBUS2_CLOCK	ABE_MCASP_AXR	GPIO_121		DMTIMER11_PWM_EVT
189	**KPD_COL3**	KPD_COL0	CAM2_D0	GPIO_171		
191	**KPD_COL2**	KPD_COL5	CAM2_D10	GPIO_1		
192	**KPD_COL0**	KPD_COL3	CAM2_D3	GPIO_174		
194	**KPD_COL1**	KPD_COL4	CAM2_D8	GPIO_0		

Table 3-2 SO-DIMM 200 Pin MuX

3.3 40 PIN FFC Pin Out

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
1	JTAG_TDI	I	Data In	AE1
2	JTAG_TMS	I	Test Mode Select	AH1
3	JTAG_NTRST	I	Reset	AH2
4	JTAG_TDO	O	Data Out	AE2
5	JTAG_RTCK	O	Clock Emulation	AE3
6	H_DPM_EMU0	IO	System Trace Data/Pin Mux Table 3.4	M2
7	H_DPM_EMU1	IO	System Trace Clock/Pin Mux Table 3.4	N2
8	JTAG_TCK	O	Test Clock/Pin Mux Table 3.4	AG1
9	GND	POWER	Digital GND	A10
10	VIO	POWER	1.8V Out	A13
11	GPMC_AD0	IO	GPMC Interface /Pin Mux Table 3.4	C12
12	GPMC_AD1	IO	GPMC Interface /Pin Mux Table 3.4	D12
13	GPMC_AD2	IO	GPMC Interface /Pin Mux Table 3.4	C13
14	GPMC_AD3	IO	GPMC Interface /Pin Mux Table 3.4	D13
15	GPMC_AD4	IO	GPMC Interface /Pin Mux Table 3.4	C15
16	GPMC_AD5	IO	GPMC Interface /Pin Mux Table 3.4	D15
17	GND	POWER	Digital GND	A10
18	GPMC_AD6	IO	GPMC Interface /Pin Mux Table 3.4	A16
19	GPMC_AD7	IO	GPMC Interface /Pin Mux Table 3.4	B16
20	GPMC_AD8	IO	GPMC Interface /Pin Mux Table 3.4	C16
21	GPMC_AD9	IO	GPMC Interface /Pin Mux Table 3.4	D16
22	GPMC_AD10	IO	GPMC Interface /Pin Mux Table 3.4	C17
23	GPMC_AD11	IO	GPMC Interface /Pin Mux Table 3.4	D17
24	GND	POWER	Digital GND	A10
25	GPMC_CLK	IO	GPMC Interface /Pin Mux Table 3.4	B22
26	GPMC_AD13	IO	GPMC Interface /Pin Mux Table 3.4	D18
27	GPMC_AD12	IO	GPMC Interface /Pin Mux Table 3.4	C18
28	GPMC_AD14	IO	GPMC Interface /Pin Mux Table 3.4	C19
29	GPMC_AD15	IO	GPMC Interface /Pin Mux Table 3.4	D19
30	GND	POWER	Digital GND	A10
31	GPMC_A20	IO	GPMC Interface /Pin Mux Table 3.4	B19
32	GPMC_A21	IO	GPMC Interface /Pin Mux Table 3.4	B20
33	GPMC_A22	IO	GPMC Interface /Pin Mux Table 3.4	A21
34	GPMC_NCS2	IO	GPMC Interface /Pin Mux Table 3.4	D21
35	GPMC_NCS1	IO	GPMC Interface /Pin Mux Table 3.4	C21
36	GND	POWER	Digital GND	A10
37	GPMC_NADV_AL	IO	GPMC Interface /Pin Mux Table 3.4	D25

Pin #	Pin Name	Type	Pin Group	OMAP 4 Ball
	E			
38	GPMC_NOE	IO	GPMC Interface /Pin Mux Table 3.4	B11
39	GPMC_NWE	IO	GPMC Interface /Pin Mux Table 3.4	B12
40	GPMC_NBE0_CLE	IO	GPMC Interface /Pin Mux Table 3.4	C23

Table 3-3 40 Pin FFC Pin Out

3.4 40 PIN FPC Pin Mux

The table below summarizes the additional available functionality for each pin of the 40-pin FPC connector. Default pin mode is marked in bold.

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
6	dpm_emu0			gpio_11		
7	dpm_emu1			gpio_12		
11	gpmc_ad0	sdmmc2_dat0				
12	gpmc_ad1	sdmmc2_dat1				
13	gpmc_ad2	sdmmc2_dat2				
14	gpmc_ad3	sdmmc2_dat3				
15	gpmc_ad4	sdmmc2_dat4	sdmmc2_dir_dat0			
16	gpmc_ad5	sdmmc2_dat5	sdmmc2_dir_dat1			
18	gpmc_ad6	sdmmc2_dat6	sdmmc2_dir_cmd			
19	gpmc_ad7	sdmmc2_dat7	sdmmc2_clk_fdbk			
20	gpmc_ad8	kpd_row0	c2c_data15	gpio_32		sdmmc1_dat0
21	gpmc_ad9	kpd_row1	c2c_data14	gpio_33		sdmmc1_dat1
22	gpmc_ad10	kpd_row2	c2c_data13	gpio_34		sdmmc1_dat2
23	gpmc_ad11	kpd_row3	c2c_data12	gpio_35		sdmmc1_dat3
25	gpmc_clk			gpio_55	sys_ndmareq2	sdmmc1_cmd
26	gpmc_ad13	kpd_col1	c2c_data10	gpio_37		sdmmc1_dat5
27	gpmc_ad12	kpd_col0	c2c_data11	gpio_36		sdmmc1_dat4
28	gpmc_ad14	kpd_col2	c2c_data9	gpio_38		sdmmc1_dat6
29	gpmc_ad15	kpd_col3	c2c_data8	gpio_39		sdmmc1_dat7
31	gpmc_a20	kpd_col4	c2c_datain4	gpio_44	venc_656_data4	
32	gpmc_a21	kpd_col5	c2c_datain5	gpio_45	venc_656_data5	
33	gpmc_a22	kpd_col6	c2c_datain6	gpio_46	venc_656_data6	
34	gpmc_ncs2	kpd_row8	c2c_dataout7	gpio_52		
35	gpmc_ncs1		c2c_dataout6	gpio_51		
37	gpmc_nadv_ale	dsi1_te1		gpio_56	sys_ndmareq3	sdmmc1_clk
38	gpmc_noe	sdmmc2_clk				
39	gpmc_nwe	sdmmc2_cmd				
40	gpmc_nbe0_cle	dsi2_te0		gpio_59		

Table 3-4 40-PIN FPC Pin Mux

4 Interface Details

4.1 Overview

This chapter describes in detail the VAR-SOM-OM44 interfaces, referring to the default SoM pin names. However, many additional interfaces are available when different pin modes are selected by the user. For example, the McSPI2 bus is available to the user when the McBSP2 pin mode is set to '1'. Tables 3 - 2 and 3 - 4 (SO-DIMM200 /40-PIN FPC Pin Mux) detail the additional possible options for each pin on the VAR-SOM-OM44 connectors.

The following list describes this chapter's column header tables:

Signal:
VAR-SOM-OM44 original pin name

Pin#:
Pin Number on the SO-DIMM200 connector (excluding GPMC & JTAG interfaces which are exposed by the 40-pin FCC connector)

Type:
Pin Type & Direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Description:
Short Pin functionality description

4.2 Display Interfaces

4.2.1 Overview

The VAR-SOM-OM44 provides the logic to display a video frame from the memory frame buffer on an LCD panel or a TV set
The primary LCD output:

- DSI1 (MIPI® DSI) – SXGA(1400x1050) VESA timing @ 60 FPS

The secondary LCD:

- Parallel RGB output (MIPI DPI 1.0) - SXGA (1400x1050) VESA timing @ 85 fps1080i/720p

HDMI interface:
High-Definition Multimedia Interface (using TV set out) - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI

4.2.2 DPI (Display Parallel Interface)

4.2.2.1 DPI Features

Panel supported with MIPI DPI protocol:

- 4/8-bit monochrome passive matrix panel interface support (15 gray scale levels supported using dithering block)
- 8-bit color passive matrix panel interface support (3375 colors supported for a color panel using dithering block)
- 12/16/18/24-bit active matrix panel interface support

4.2.2.2 DPI Signals

Signal	Pin #	Type	Description
DISPC2_PCLK	28	O	DPI Pixel Clock
DISPC2_HSYNC	26	O	DPI Horizontal Sync
DISPC2_VSYNC	46	O	DPI Vertical Sync
DISPC2_DE	64	O	DPI Data Enable
DISPC2_DATA0	66	O	DPI Data Line 0
DISPC2_DATA1	68	O	DPI Data Line 1
DISPC2_DATA2	4	O	DPI Data Line 2
DISPC2_DATA3	3	O	DPI Data Line 3
DISPC2_DATA4	6	O	DPI Data Line 4
DISPC2_DATA5	5	O	DPI Data Line 5
DISPC2_DATA6	8	O	DPI Data Line 6
DISPC2_DATA7	7	O	DPI Data Line 7
DISPC2_DATA8	70	O	DPI Data Line 8
DISPC2_DATA9	62	O	DPI Data Line 9
DISPC2_DATA10	12	O	DPI Data Line 10
DISPC2_DATA11	11	O	DPI Data Line 11
DISPC2_DATA12	14	O	DPI Data Line 12
DISPC2_DATA13	13	O	DPI Data Line 13
DISPC2_DATA14	16	O	DPI Data Line 14
DISPC2_DATA15	15	O	DPI Data Line 15
DISPC2_DATA16	45	O	DPI Data Line 16
DISPC2_DATA17	17	O	DPI Data Line 17
DISPC2_DATA18	20	O	DPI Data Line 18
DISPC2_DATA19	19	O	DPI Data Line 19
DISPC2_DATA20	22	O	DPI Data Line 20
DISPC2_DATA21	21	O	DPI Data Line 21
DISPC2_DATA22	24	O	DPI Data Line 22
DISPC2_DATA23	23	O	DPI Data Line 23

Table 4-1 DPI Signals

4.2.3 DSI1Display Serial Interfaces

The DSI1 interface is not supported by default VAR-SOM-OM44 configuration. Contact support@varisicte.com for more information.

4.2.4 HDMI

4.2.4.1 HDMI Features

Driven by the native OMPA4460 HDMI interface, the list below summarizes HDMI interface features:

- HDMI 1.3, HDCP 1.2, and DVI 1.0 compliant, including support for the 3D stereoscopic frame-packing formats of the HDMI v1.4 standard (720p, 50 Hz; 720p, 60 Hz; and 1080p, 24 Hz)
- EIA/CEA-861-D video format support (refer to Table 10 - 628 for more details)
- VESA DMT video format support (refer to Table 10 - 629 for more details)
- Support for deep-color mode:
  - 10-bit/component color depth up to 1080p @60 Hz
  - 12-bit/component color depth up to 720p/1080i @60 Hz
- Supports up to 148.5 MHz pixel clock (1920 x 1080p @60 Hz)
- Video formats: 24-bit RGB
- Uncompressed multi-channel (up to 8-channels) audio (L-PCM) support
- Master I2C interface for Display Data Channel (DDC) connection
- Consumer Electronic Control (CEC) interface
- Integrated High-bandwidth Digital Content Protection (HDCP) encryption engine for transmitting protected audio and video content (authentication performed by software)
- Integrated Transition Minimized Differential Signaling (TMDS) and TMDS Error Reduction Coding (TERC4) encoders for data island support
- Integrated TMDS PHY (3 TMDS differential data lanes + TMDS differential clock lane)
  – Up to 1,85625 Gbps per lane at (1080p @60 Hz at 10-bit/component, lower resolutions at 12-bit/component)
  – 928,125Mbps per lane at (720p/1080i @60 Hz 10-bit/component, lower resolutions at 12-bit/component)

4.2.4.2 HDMI Signals

Signal	Pin #	Type	Description
HDMI_CLOCKX	150	ODS	HDMI Clock Differential
HDMI_CLOCKY	148	ODS	HDMI Clock Differential
HDMI_DATA0X	149	ODS	HDMI Data 0 Differential
HDMI_DATA0Y	147	ODS	HDMI Data 0 Differential
HDMI_DATA1X	142	ODS	HDMI Data 1 Differential
HDMI_DATA1Y	144	ODS	HDMI Data 1 Differential
HDMI_DATA2X	155	ODS	HDMI Data 2 Differential
HDMI_DATA2Y	157	ODS	HDMI Data 2 Differential
HDMI_DDC_SCL	154	IO	Display Data Channel Clock
HDMI_DDC_SDA	153	IO	Display Data Channel Data
HDMI_HPD	160	I	Hot Plug Detect
HDMI_CEC	152	IO	Consumer Electronic Control

Table 4-2 HDMI Signals

4.3 Camera Interfaces

The VAR-SOM-OM44 features three camera interfaces:

- 16-bit CPI (Camera Parallel Interface)
- 2 X CSI2 (Camera Serial Interface)

Note: The serial camera interface signals are muxed with camera parallel interface signals.

4.3.1 Camera Interface Features

CPI (Camera Parallel Interface):

- 16-bit wide
- Up to 148.5 MPix/s
- BT656 and SYNC mode (HS, VS, FIELD, WEN)

CSI (Camera Serial Interface):

CSI2 camera interfaces

- Transfer pixels and data received by the CSI2 digital physical layer receiver to the system memory or to the ISP
- Use unidirectional data link
- CSI2-A supports four configurable data links in addition to the clock signaling
- CSI2-B supports two configurable data links in addition to the clock signaling
- Maximum data rate of 1 Gbps per data lane
- Data merger for 2, 3, or 4-data lane configuration
- Maximum data rate of 1 Gbps per data lane, possible configurations are:
    - One data lane: 1000 Mbps (824 Mbps if lane 4 is used)
    - Two data lanes: 2 × 1000 Mbps (2 × 824 Mbps if lane 4 is used
    - Three data lanes: 3 × 1000 Mbps (3 × 824 Mbps if lane 4 is used)
    - Four data lanes: 4 × 824 Mbps
- Error detection and correction by the protocol engine
- Direct Memory Access (DMA) engine integrated with dedicated First In First Out (FIFO)
- 1-Dimensional (1D) and 2-Dimensional (2D) addressing mode
- Burst support
- Streaming burst support (64 or 32-bit)
- Eight contexts to support eight dedicated configurations of virtual channel ID and data types
- Ping-pong mechanism for double-buffering
- All primary and secondary MIPI-defined formats are supported
- Conversion of the RGB formats
- On-the-fly differential pulse code modulation (DPCM) decompression
- On-the-fly image cropping and A-law/DPCM compression

CCP2 camera interface (secondary)

- Four logical channels
- Transfer pixels and data received by the complex I/O PHY (CCP2 D-PHY RX to the system memory or the ISP)
- Use unidirectional data link
- Maximum data rate of 650 Mbps
- DMA engine integrated with dedicated FIFO
- 1D and 2D addressing mode
- False synchronization code protection
- Ping-pong mechanism for double-buffering
- RGB, RAW, YUV, and JPEG formats supported
- On-the-fly DPCM decompression
- On-the-fly image cropping and A-Law/DPCM compression

4.3.2 CPI Signals

Signal	Pin #	Type	Description
CAM2 _PCLK	59	I	Parallel Interface Pixel Clock
CAM2 _HS	72	IO	Line Trigger Input/output Signal
CAM2 _VS	80	IO	Frame Trigger Input/output Signal
CAM2 _FLD	138	IO	Field Identification Input/output Signal
CAM2 _WEN	136	I	External Write-enable Signal
CAM _STROBE	35	O	Flash Strobe Control Signal
CAM2_D0	189	I	ISP Data (LSB)
CAM2 _D1	182	I	ISP Data
CAM2 _D2	180	I	ISP Data
CAM2 _D3	192	I	ISP Data
CAM2 _D4	85	I	ISP Data
CAM2 _D5	129	I	ISP Data
CAM2 _D6	55	I	ISP Data
CAM2 _D7	78	I	ISP Data
CAM2 _D8	194	I	ISP Data
CAM2 _D9	76	I	ISP Data
CAM2 _D10	191	I	ISP Data
CAM2 _D11	87	I	ISP Data
CAM2 _D12	141	I	ISP Data
CAM2 _D13	143	I	ISP Data
CAM2 _D14	135	I	ISP Data
CAM2 _D15	137	I	ISP Data (MSB)

Table 4-3 CPI Signals

CSI21 Signals

Signal	Pin #	Type	Description
CSI21_DX0	50	IDS	CSI2 (CSI21) Camera Lane 0 differential x
CSI21_DY0	52	IDS	CSI2 (CSI21) Camera Lane 2 Differential Y
CSI21_DX1	130	IDS	CSI2 (CSI21) Camera Lane 0 Differential X
CSI21_DY1	132	IDS	CSI2 (CSI21) Camera Lane 3 Differential Y
CSI21_DX2	56	IDS	CSI2 (CSI21) Camera Lane 1 Differential X
CSI21_DY2	54	IDS	CSI2 (CSI21) Camera Lane 3 Differential Y
CSI21_DX3	53	IDS	CSI2 (CSI21) Camera Lane 1 Differential X
CSI21_DY3	55	IDS	CSI2 (CSI21) Camera Lane 4 Differential Y
CSI21_DX4	129	IDS	CSI2 (CSI21) Camera Lane 2 Differential X
CSI21_DY4	131	IDS	CSI2 (CSI21) Camera Lane 4 Differential Y

Table 4-4 CSI21 Signals

4.3.3 CSI22 Signals

Signal	Pin #	Type	Description
CSI22_DX0	141	IDS	CSI2 (CSI22) Camera Lane 0 Differential X
CSI22_DY0	143	IDS	CSI2 (CSI22) Camera Lane 0 Differential Y
CSI22_DX1	135	IDS	CSI2 (CSI22) Camera Lane 0 Differential X
CSI22_DY1	137	IDS	CSI2 (CSI22) Camera Lane 0 Differential Y
CSI22_DX2	138	IDS	CSI2 (CSI22) Camera Lane 0 Differential X
CSI22_DY2	136	IDS	CSI2 (CSI22) Camera Lane 0 Differential Y

Table 4-5 CSI22 Signals

4.4 Gigabit Ethernet

4.4.1 Gigabit Ethernet Features

Based on the SMSC LAN7500, VAR-SOM-OM44 Gigabit Ethernet interface features:

- Fully compliant with IEEE802.3/802.3u/802.3ab
- Integrated Ethernet MAC and PHY with HP Auto-MDIX
- 10BASE-T, 100BASE-TX, and 1000BASE-T support
- NetDetach provides automatic USB attach/detach when the Ethernet cable is connected/removed
- Full and half-duplex capability (only full-duplex operation at 1000 Mbps)
- Full-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- 9 KB jumbo frame support
- Automatic payload padding and pad removal
- Loop-back modes
- Supports checksum offloads (IPv4, IPv6, TCP, UDP)
- Supports Microsoft NDIS 6.2 large send offload
- Supports IEEE 802.1q VLAN tagging
- Ability to add and strip IEEE 802.1q VLAN tags
- VLAN tag based packet filtering (all 4096 VIDs)

4.4.2 Gigabit Ethernet Magnetics

In order to utilize the VAR-SOM-OM44 Gigabit Ethernet interface, compatible magnetics should be used on the carrier board. SMSC defines the below magnetics options:

Magnetics listed under a “Qualified” title have been tested by SMSC in order to verify the proper operation with the LAN7500 device. Magnetics in the “suggested” category were evaluated on the vendor-supplied datasheet level, but have not been tested.

Qualified Magnetics:

Vendor	Part Number	Package	Cores	Temp.	Configuration
Halo	HFJ11-1G02E	Integrated RJ45	8	0 C° – +70 C°	HP Auto-MDX

Suggested Magnetics:

Vendor	Part Number	Package	Cores	Temp	Configuration
Halo	TG1G-S002NZRL	24-pin SOIC-W	8	0 C° – +70 C°	HP Auto-MDX

Note: Please refer to SMSC application notes for the most up-to-date and detailed information regarding qualified and suggested Magnetics.
http://www.smsc.com/media/Downloads/Application_Notes/an813.pdf

4.4.3 Gigabit Ethernet Signals

Signal	Pin #	Type	Description
GETH_TXN	165	IODS	Bi-directional Pair Negative, 10/100 Mbps Tx Backwards Compatibility
GETH_TXP	167	IODS	Bi-directional Pair Positive, 10/100 Mbps Tx Backwards Compatibility
GETH_RXN	171	IODS	Bi-directional Pair Negative, 10/100 Mbps Rx Backwards Compatibility
GETH_RXP	173	IODS	Bi-directional Pair Positive, 10/100 Mbps Rx Backwards Compatibility
GETH_D2N	177	IODS	Bi-directional Pair Negative
GETH_D2P	179	IODS	Bi-directional Pair Positive
GETH_D3N	183	IODS	Bi-directional Pair Negative
GETH_D3P	185	IODS	Bi-directional Pair Positive
LINK_LED	161	IODS	Activity Indicator
LINK_SPEED	163	IODS	Speed Indicator

Table 4-6 Ethernet Signals

4.5 Wi-Fi & Bluetooth

Wi-Fi & Bluetooth connectivity is supported by on board Murata LBEH59XUHC, a IEEE802.11 b/g/n + Bluetooth 4.0 module based on TI's WL1271L chipset.

J4 is a U.FL connector for an external antenna connection, serves both Wi-Fi & Bluetooth modules.

4.6 USB HOST 2.0

Two USB2.0 host interfaces are supported, featured by an on-board USB 2.0 HUB.

4.6.1 USB Host1 Signals

Signal	Pin #	Type	Description
USBHOST_DP1	103	IODS	USB Host Data Positive
USBHOST_DN1	105	IODS	USB Host Data Negative
USBHOST_PWORCTRL1	107	I	USB Host Over Current Indicator – External Pull-up Required

Table 4-7 USB HOST1 Signals

4.6.2 USB Host2 Signals

Signal	Pin #	Type	Description
USBHOST2_DP	121	IODS	USB Host Data Positive
USBHOST2_DN	123	IODS	USB Host Data Negative
USBHOST2__PWORCTRL2	111	I	USB Host Over Current Indicator – External Pull-up Required

Table 4-8 USB HOST2

4.7 USB 2.0 On-The-Go

4.7.1 USB 2.0 On-The-Go Features

The OMAP4460 High-Speed USB controller is a high-speed, USB OTG dual-role-device (DRD) link controller supporting the following modes:

- USB 2.0 peripheral (function controller) in high/full speed (480/12 Mbps, respectively)
- USB 2.0 host in high/full/low speed (480/12/1.5 Mbps, respectively), with one downstream port but multipoint capability when a hub is connected to it (split transaction support etc.)
- USB 2.0 OTG DRD in high/full speed, with HNP (OTG1.3) and SRP support

4.7.2 OTG Signals

Signal	Pin #	Type	Description
USB_OTG_DN	122	IODS	USB OTG Data Negative
USB_OTG_DP	120	IODS	USB OTG Data Positive
USB_OTG_VBUS	118	I	USB 2.0 OTG VBUS indicator (5V)

USB_OTG_ID	124	I	USB OTG Host/Client ID Low : Host Mode Float: Client Mode

Table 4-9 USB OTG Signals

Note: In host mode, an external regulator is required to supply the USB bus voltage to the connected device(s).

4.8 MMC/SD/SDIO

By default, two 1.8 V, 4-bit MMC/SD/SDIO interfaces are supported, MMC/SD/SDIO2 and MMC/SD/SDIO4. MMC/SD/SDIO2 can be used as boot device. MMC/SD/SDIO4 is only available if on-board Wi-Fi connectivity is not used.

4.8.1 MMC/SD/SDIO Features

Compliance with standards:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MC/eMMC Standard Specification v4.41, including high-capacity (size 2 GB) cards HC MMC
- Full compliance with SD command/response sets as defined in the SD Specifications Part 1 Physical Layer Simplified Specification v3.01, including high-capacity SDHC cards up to 32 GB
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations, as defined in the SDIO Card Specification Part E1, v2.00
- Full compliance with sets as defined in the SD Card Specification Part A2, SD Host Controller Standard Specification v2.00
- Full compliance with MMC bus testing procedure as defined in the Multimedia Card System Specification v4.41
- Full compliance with CE-ATA command/response sets as defined in the CE-ATA Standard Specification
- Full compliance with ATA for MMCA specification
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the CE-ATA Standard Specification

Main features of the MMC/SD/SDIO host controller:

- Flexible architecture allowing support for a new command structure
- Support:
  - 1 or 4-bit transfer mode specifications for SD and SDIO cards
  - 1, 4, or 8-bit transfer mode specifications for MMC cards
- Built-in buffer for read or write (up to 2048 bytes in single-buffering, 1024 bytes in double-buffering)
- 32-bit wide access bus to maximize bus throughput
- Single interrupt line for interrupt source events
- Two slave DMA channels (one for TX, one for RX)

- Designed for low power
- Programmable clock generation
- Support SDIO read wait and suspend/resume functions
- Support stop at block gap
- Support boot mode operations as specified in the JEDEC JC 64 MMC/eMMC Standard Specification v4.41
- Support Dual Data Rate transfers (DDR mode) as specified in JEDEC JC64 MMC/eMMC Standard Specification v4.41
- Support SDA 2.0 Part A2 programming model optional features (depending on module integration):
    - Master interface (Level 3 [L3] interconnect)
    - One master DMA (32-bit ADMA2), replacing the two slave DMA channels
- Retention mode is supported
- Supported clock frequencies:

MMC mode:
- Up to 48 MHz in DDR and SDR modes

SD mode:
- Up to 48 MHz in DDR mode
- Up to 96 MHz in SDR mode

SDIO mode:
- Up to 48 MHz in SDR mode

4.8.2 SDMMC2 Signals

Signal	Pin #	Type	Description
MMC2_DAT0	36	IO	MMC2 Data
MMC2_DAT1	38	IO	MMC2 Data
MMC2_DAT2	40	IO	MMC2 Data
MMC2_DAT3	42	IO	MMC2 Data
MMC2_CLKO	32	O	MMC Clock
MMC2_CMD	43	O	MMC Command

Table 4-10 SDMMC2 Signals

4.8.3 SDMMC4 Signals

Signal	Pin #	Type	Description
MMC4_DAT0	168	IO	MMC4 Data
MMC4_DAT1	170	IO	MMC4 Data
MMC4_DAT2	172	IO	MMC4 Data
MMC4_DAT3	174	IO	MMC4 Data
MMC4_CLK	164	O	MMC4 Clock
MMC4_CMD	166	O	MMC4 command

Table 4-11 SDMMC4 Signals

Note: MMC4 Signals are shared with the on board Wi-Fi module

4.9 Audio

The VAR-SOM-OM44 features four audio interfaces

- Stereo line in
- Stereo Headphones driver
- Digital microphone
- S/PDIF out

4.9.1 Audio Features

4.9.1.1 Analog

Analog audio signals are featured by an on-board TWL6040 audio codec device. Please refer to the TWL6040 data sheet for detailed electrical characteristics of relevant interfaces.

http://www.ti.com/lit/ds/symlink/twl6040.pdf

4.9.1.2 Digital Microphone

- Microphone is directly connected to the TX filter decimator to extract the audio samples with a maximum of 96 db SNR at a frequency sampling set to 96 kHz.
- Supports idle request/acknowledge protocol
- Rising or falling edge configuration for the clock signal sampling
- DMIC-clock-programmable
- Interconnect slave interface (internal interconnect) supports 32-bit data bus width.
- One DMA request capability on a programmable FIFO threshold
- One RX FIFO (16-bit x 24-bit word depth)
- Complies with PRCM interrupts to the Cortex-A9 MPU and DSP subsystems
- Interconnect sample format: 32-bits (only 24 are significant)
- Supports idle request/acknowledge PRCM protocol

4.9.1.3 S/PDIF

- Support of the idle request/acknowledge protocol
- Buffer for transmit operations
- One transmit Direct Memory Access (DMA) request linked with a 32-bit register and one transmit interrupt request
- One transmit channel
- One serializer

4.9.1.4 Audio Signals

Signal	Pin #	Type	Description
HP_OUT_L	198	AO	Pre-amped Headphones, Left Out
HP_OUT_R	200	AO	Pre-amped Headphone, Right Out
AUDIO_IN_L	197	AI	Line In, Left Channel

AUDIO_IN_R	199	AI	Line In, Right Channel
DMIC_CLK	186	O	Digital Microphone Clock
DMIC_DATA	188	I	Digital Microphone Data
S/PDIF	102	O	S/PDIF Out Muxed with MCBSP2_DR
AUD_GND	195, 196	Power	Audio Ground

Table 4-12 Audio Signals

4.10 UART Interfaces

By default three UART interfaces are supported, refer to Table 3.2 for further configuration options for the UART interface.

4.10.1 UART Features

Main features of VAR-SOM-OM44 UARTS:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable baud rate generator up to 3.6 Mbits
- Programmable interrupt trigger levels for FIFOs
- Break character detection and generation
- Configurable data format:
  - Data bits: 5, 6, 7, or 8-bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2-bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

Receive and transmit FIFO fill and drain operations can be done using programmed IO or DMA transfers. To minimize CPU overhead for UART communications, device driver software can setup interrupts and DMA for data transfers to/from memory.

4.10.2 UART1 Signals

Signal	Pin #	Type	Description
UART1_TX	84	O	UART Transmit
UART1_RX	90	I	UART Receive
UART1_RTS	86	O	UART HW Flow Control RTS
UART1_CTS	88	I	UART HW Flow Control CTS

Table 4-13 UART1 Signals

4.10.3 UART2 Signals

Signal	Pin #	Type	Description
UART2_TX	69	O	UART Transmit
UART2_RX	71	I	UART Receive
UART2_RTS	67	O	UART HW Flow Control RTS
UART2_CTS	65	I	UART HW Flow Control CTS

Table 4-14 UART2 Signals

Note: UART2 Signals are shared with an on board Bluetooth connectivity device.

4.10.4 UART3 Signals

Signal	Pin #	Type	Description
UART3_TX	35	O	UART Transmit
UART3_RX	33	I	UART Receive
UART3_RTS	31	O	UART HW Flow Control RTS
UART3_CTS	29	I	UART HW Flow Control CTS

Table 4-15 UART3 Signals

Note: UART3 is used as default boot debug port.

4.11 Multi-channel Buffered Serial Ports

The Multi-channel Buffered Serial Ports (McBSP) provide a full-duplex direct serial interface between the device and other devices in a system such as audio and voice codecs. VAR-SOM-OM44 supports McBSP in a 4-pin configuration (CLKR and FSR are connected internally to CLKX and FSX respectively). By default two McBSP (McBSP1, McBSP2) interfaces are supported, refer to Table 3.2 for further McBsP interfaces configuration options.

4.11.1 McBSP Features

The main features of the McBSP modules are:

- L4 interconnect slave interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 16/8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write non-posted transaction mode supported
- 128 × 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Transmit and receive Direct Memory Access (DMA) requests triggered with programmable FIFO thresholds
- Serial interface description
  - 6-pin configuration (McBSP 4 only)
  - 4-pin configuration (McBSP1, 2, 3)
  - Full-duplex communication
  - Multichannel selection modes
- Support to enable or block transfers in each channel
- 128 channels for transmission and reception
  - Direct interface to industry-standard codecs, Analog Interface Chips (AICs), and other serially
- Connected A/D and D/A devices:
  - Inter-IC sound (I2S™) compliant devices
  - Pulse Code Modulation (PCM) devices
  - Time Division Multiplexed (TDM) bus devices
  - A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
  - Bit reordering (send/receive Least Significant Bit [LSB])
- Clock and frame-synchronization generation support:
  - Independent clocking/framing for reception and transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable Sample Rate Generator (SRG) for internal generation and control of clock signals and frame-sync signals
  - Programmable polarity for frame-sync pulses and clock signals

4.11.2 McBSP1Signals

Signal	Pin #	Type	Description
McBSP1_CLKX	27	IO	McBSP Transmit Clock
McBSP1_FSX	93	IO	McBSP Transmit Frame Synchronization
McBSP1_DR	176	I	McBSP Receive Serial Data

McBSP1_DX	95	(I)O	McBSP Transmit Serial Data

Table 4-16 McBSP1 Signals

4.11.3 McBSP2 Signals

Signal	Pin #	Type	Description
McBSP2_CLKX	98	IO	McBSP Transmit Clock
McBSP2_FSX	106	IO	McBSP Transmit Frame Synchronization
McBSP2_DR	102	I	McBSP Receive Serial Data
McBSP2_DX	104	(I)O	McBSP Transmit Serial Data

Table 4-17 McBSP2 Signals

4.12 SPI

The VAR-SOM-OM44 SPI is based on OMAP4 McSPI x. By default one McSPI (McSPI1) interface is supported. Refer to Table 3.2 for further McSPI interfaces configuration options.

4.12.1 SPI Features

The SPI interface includes the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32-bits
- Up to four master channels, or a single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible I/O port controls per channel
  - Two DMA requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- 64-byte built-in FIFO available for a single channel
- Force CS mode for continuous transfers

4.12.2 McSPI1 Signals

Signal	Pin #	Type	Description
McSPI1_CLK	37	IO	MsSPI1 Clock
McSPI1_SIMO	39	IO	MsSPI1 SIMO Signal
McSPI1_SOMI	41	IO	MsSPI1 MISO Signal
McSPI1_CS0	34	IO	MsSPI1 Chip Select 0 Signal

Table 4-18 SPI Signals

4.13 I²C

By default, two I²C (I2C3, I2C4) interfaces are supported, driven by the OMAP4460 controller. Refer to Table 3.2 for further configuration options for I²C interfaces.

4.13.1 I²C Features

OMAP4 I²C controller main features are:

- Compliant with Philips I²C specification version 3.0
- Supports standard mode (up to 100 Kbps), fast mode (up to 400 Kbps), and fast mode+ (up to 1 Mbps)
- Supports HS mode for transfer up to 3.4 Mbps
- Support for 3-wire/2-wire SCCB master mode for I2C2 and I2C3 modules, 2-wire SCCB master mode for I2C1 and I2C4 modules, up to 100 Kbps
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multi-master transmitter/slave receiver mode
- Multi-master receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in configurable FIFO (8, 16, 32, 64-bytes) for buffered read or write
- Module enable/disable capability
- Programmable multi-slave channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Open-core protocol (OCP) interface with LH application (OCP-IP 2.0 compliant)
- Designed for low power consumption
- Implement auto idle mechanism
- Implement idle Request/idle acknowledge handshake mechanism
- Support for asynchronous wake-up mechanism
- Two Direct Memory Access (DMA) channels
- Wide interrupt capability
- Supports OmniVision SCCB protocol
- Compliant with Highlander 0.8

The master transmitter HS I2C controller I2C5 has the following features:

- Support of HS and fast modes
- 7-bit addressing mode only
- Master transmitter mode only
- Start/restart/stop

4.13.2 I2C3 Signals

Signal	Pin #	Type	Description
I2C3_SCL	63	IO	I2C3 I^{2}C Clock , Open Drain
I2C3_SDA	61	IO	I2C3 I^{2}C Data, Open Drain

Table 4-19 I2C3 Signals

Note: I2C3 interface is used by some on board devices. Pin configuration for I2C3 signal can't be changed.

4.13.3 I2C3 Address Mapping

The table below summarizes I2C3 address used by on board I^{2}C slave devices:

Device	Address
Touch Controller	0x1001000_R/W
Temperature Sensor	0x1001001_ R/W
EEPROM	0x1010000_ R/W

Table 4-20 I2C3 Address Mapping

4.13.4 I2C4 Signals

Signal	Pin #	Type	Description
I2C4_SCL	101	IO	I2C4 I^{2}C Clock, Open Drain
I2C4_SDA	99	IO	I2C4 I^{2}C Data, Open Drain

Table 4-21 I2C4 Signals

4.14 HDQ/1-Wire

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmark HDQ and Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slave (HDQ/1-Wire external compliant device).
A typical application of the HDQ/1-Wire is the communication with battery monitor (gas gauge) integrated circuits.

4.14.1 1-Wire / HDQ Feature

The HDQ/1-Wire provides a communication rate of 5 Kbps over an address space of 128 bytes.

4.14.2 1-Wire / HDQ Signal

Signal	Pin #	Type	Description
HDQ	82	IO	HDQ / 1-Wire IO Signal

Table 4-22 HDQ Signal

4.15 PWM0

By default, one PWM interface is supported, driven by the OMAP4460 controller, refer to Table 3.2 for further configuration options for PWM (under "DMTIMERX_PWM_EVT" functions).

4.15.1 PWM0 Signal

Signal	Pin #	Type	Description
PWM0	158	O	PWM Signal (in mode 5)

Table 4-23 PWM0 Signal

4.16 Local Bus

The General Purpose Memory Controller (GPMC) is used to interface external memory devices:

- SRAMs
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flashes
- Pseudo-SRAM devices

Most of OMAP4 local bus (GPMC) signals are available through VAR-SOM-OM44 40 pin FPC connector described above in the “SoM Connectors” section 3, Table 3.3.

4.17 Touch Screen

VAR-SOM-OM44 features a native, 4-wire resistive touch panel interface based on Texas Instrument's TSC2004 device.

4.17.1 Touch Screen Controller Features

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

4.17.2 Touch-screen Controller Signals

Signal	Pin #	Type	Description
TSMX	77	AI	Touch Screen X Minus
TSMY	79	AI	Touch Screen Y Minus
TSPX	73	AI	Touch Screen X Plus
TSPY	75	AI	Touch Screen Y Plus

Table 4-24 Touch Panel Signals

4.18 Keypad

VAR-SOM-OM44 keypad interface is based on the OMAP4 keypad controller, not every OMAP4 keypad IO is supported by VAR-SOM-OM44. See the table below for more details.

4.18.1 Keypad Controller Features

The keyboard controller includes the following main features:

- Support of multi-configuration keyboards up to 3 rows × 6 columns
- Each key coded on 1-bit in two 32-bit registers
- Long-key value or repeat timing reconfigurable on-the-fly
- Event detection on key press and key release
- Multi-key-press detection and decoding
- Long-key detection on prolonged key press
- Integrated timer with four programmable comparison values
- Programmable time-out on permanent key press or after keyboard release
- Programmable interrupt generation on key events
- Software reset capability

The keyboard controller detects and decodes multi-key combinations using the following rules:

- Any 2-key combination is valid and can be decoded
- Combinations using more than two keys are valid only if the rows and columns used do not cross over another key that is to be detected. This is caused by equipotent propagation on a row/column (multi-key limitations).

4.18.2 Keypad Controller Signals

Signal	Pin #	Type	Description
KPD_RAW0	78	I	Keypad Row
KPD_RAW1	76	I	Keypad Row
KPD_RAW2	87	I	Keypad Row
KPD_RAW3	85	I	Keypad Row
KPD_COL0	192	O	Keypad Column
KPD_COL1	194	O	Keypad Column
KPD_COL2	191	O	Keypad Column
KPD_COL3	189	O	Keypad Column
KPD_COL4	182	O	Keypad Column
KPD_COL5	180	O	Keypad Column

Table 4-25 Keypad Signals

4.19 General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs.
See Chapter 3, Table 3.2 and 3.4 for a complete SoM connectors signal list and GPIO multiplexing.

4.20 General System Control

4.20.1 Boot Options

The boot option signal configures the boot sequence of the VAR-SOM-OM44:
Not Connected: Boot device is an on board SD Card (using MMC/SD/SDIO1 interface), if failed, UART is used as a boot device.
Logic '1': boot device is an off board SD Card (using MMC/SD/SDIO2 interface), if failed, UART is used as a boot device.

4.20.2 Reset

'0' logic will reset major VAR-SOM-OM44 components:

- OMAP44660
- TWL6030 - PMIC
- TWL6040 – Audio Codec

4.20.3 Reference Clock Out

An OMAP4 output clock is controlled by the SCRM module. Please contact Variscite for further information regarding the configuration option for this clock.

4.20.4 General System Control Signals

Signal	Pin #	Type	Description
SYS_BOOT	92	I	System Boot Option Select [High – Internal Device Boot]
RESET_IN_N	127	I	Hardware Reset
FREF_CLK1_OUT	49	O	General Purpose Clock Out

Table 4-26 General System Signals

4.21 Power

4.21.1 Power Supply

Signal	Pin #	Type	Description
VBAT_SOM	100,108,110,112,113,114,115, 116	Power In	VAR-SOM-OM44 Single DC-IN Supply Voltage. Voltage Range: 3.3 +/- 5%
VIO	117	Power Out	1.8V Output, up to 200 mA
RTC_BACKUP	126	Power In	RTC Backup Battery Power Supply, Max : 8uA@ RTC_BACKUP = 3.2V ,VBAT =0,

Table 4-27 Power Supply Pins

4.21.2 Ground

Signal	Pin #	Type	Description
GND	1,2,9,10,18,25,30,47,48,51,57,58,60,74,81,83,94,96,119,125,128,133,134,139,140,145,146,151,156,159,162,169,175,178,181,184,187,190		Digital Ground
AGND	195,196	Power	Analog GND

Table 4-28 Ground Pins

5 Heat spreader

The VAR-SOM-OM44, based on the TI OMAP4460, is a high-performance SOM. Graphics and Video accelerators consume only ~100mW and therefore have minor effect on heat dissipation.
Most applications use the 1.5 GHz at bursts of a few seconds, upon demand. In such case there is no need for special thermal heat dissipation or heat spreader.
The heat spreader is used only for applications that continuously utilize the 1.5 GHz dual core at 100% CPU utilization.

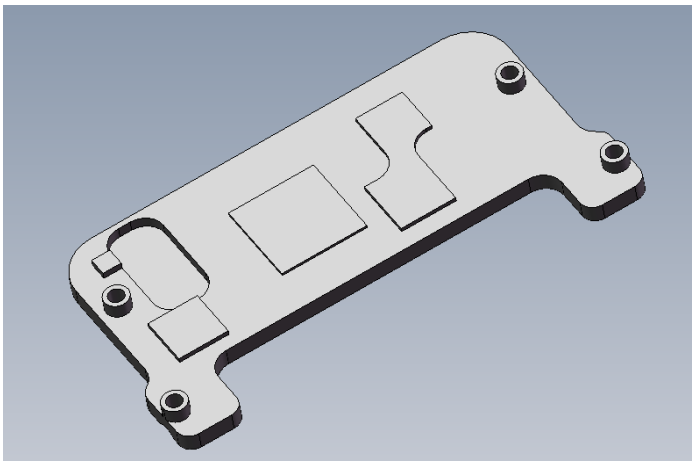
The heat spreader is required only for applications that continuously running the dual cores at high frequency, 100% CPU utilization. In this scenario, operating @ 1.5 GHz, the OMAP4 provides 7500 MIPS (higher than Intel ATOM™) and may require the use of a heat spreader.
The heat spreader can be used for mounting a proprietary heat sink or spreading the heat in any other way. It is fitted on the VAR-SOM-OM44 board top side. By thermally coupling the OMAP4460 SoC to a relatively large aluminum plain, the time period in which the VAR-SOM-OM44 can operate in a very high frequency can be extended significantly.
As part of the end-product thermal design, the customer can:

1. Use the heat spreader as is. Variscite can deliver the heat spreader in high volumes.

2. Mount a heat sink on top of the heat spreader or thermally connect it to the device casing to improve heat dissipation.

3. Design a custom head spreader. All the CAD data required for such a design is available on Variscite web site.

VAR-SOM-OM44 Bottom View



6 Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	3.5	V

Table 6-1 Absolute Maximum Characteristics

7 Operational Characteristics

7.1 Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.3	+5%	V
RTC Backup Battery Voltage	2.5	3.8	5.5	V

Table 7-1 Power Supplies Operational Characteristics

7.2 Power Consumption

The below tables summarizes the VAR-SOM-OM44 power consumption at various operational modes.

.

7.2.1 Power Consumption at various CPU utilization modes (@25°C).

Cores utilization [1]	CPU Cores Frequency [GHz]	Power [W]
Core 1 - <15% Core 2 - <15%	0.35	1.07
	0.92	1.35
	1.2	1.4
Core 1 - 100% Core 2 - < 15%	0.35	1.26
	0.92	2.05
	1.2	2.38
	1.5	2.66
Core 1 - 100% Core 2 - 100%	0.35	1.37
	0.92	2.70
	1.2	3.6
	1.5	4.185

Table 7-2-1 Power Consumption at various CPU utilization modes, 25°C

[1] 100%: CPU at full usage, running Dhrystone benchmark

7.2.2 Power Consumption at various Video & Graphics playback modes (@25°C). .

Video Playback Source	CPU Cores Frequency [GHz]	Power [W]
1080p,H.264 HD Video Playback	0.35	1.3W
1080p OpenGL 3D Graphics rendering (GLBenchmark)	0.35	1.2W

Table 7-3-2 Power Consumption at various Video & Graphics playback mode, 25°C.

8 DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
DIGITAL 1.8V IO [GPMC, DISPC,DSI,CSI, MMCx,HDQ, McBSP, HDMI_x, PDM,DMIC,SPI,UART,JTAG ,Keypad, GPIO_13, Reset]				
V_{IH}	1.17		2.1	V
V_{IL}	-0.3		0.63	V
V_{OH}	1.35			V
V_{OL}			0.45	V
I2C				
V_{IH}	1.26		2.3	V
V_{IL}	-0.5		0.54	V
V_{OH}	1.35			V
V_{OL}			0.45	V
USBHOSTx_PWORCTRL (Open Drain)				
V_{IH}	2		4.5	V
V_{IL}			0.8	V
OTG_VBUS				
Detect	2.93		3.15	V
LINK/SPEED_LED (Open Drain)				
V_{IL}			0.4	V (I_{OL}=8mA)

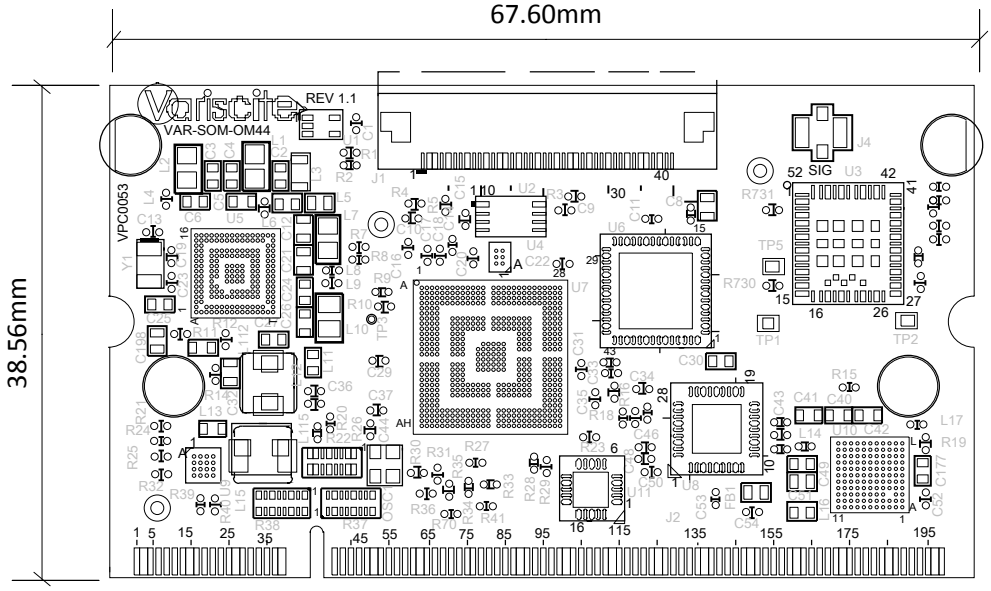
Table 8-1 DC Electrical Characteristics

9 Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-25 ^{0}C	+70 ^{0}C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 50Deg Celsius, Class B-1, GM 50Deg Celsius, Class B-1, GB	 121 Khrs > 1400 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

10 Mechanical Drawings

Top View [mm]



CAD file are available for download at http://www.variscite.com/

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